AS/A Level Computing
Syllabus 2011

Section 3

- System Software Mechanisms -

- Machine Architecture -

- Database Theory -

- Programming Paradigms -

Chapter 3.3
Computer Architectures & Fetch-Execute Cycle

3.3 Computer Architecture & Fetch-Execute Cycle

3.3.1 VON NEUMANN ARCHITECTURE

- Jon Von Neumann introduced the idea of stored programs.
- Previously, programs and data were stored in separate parts of memory.
- The idea of stored programs led to compilers that produce binary code as output.
- Von Neumann architecture uses a single processor that follows a linear sequence of Fetch-Decode-Execute.
- Main features of Von Neumann architecture:
    - Single Processor architecture.
    - Idea of stored programs.
    - Programs and data share the same (primary) memory.
    - Follows a sequential set of instructions.

3.3 Computer Architecture & Fetch-Execute Cycle

3.3.2 Registers: Purpose and Use

The processor needs special registers to perform fetch-decode-execute cycle. These are:

Register	Abbrev	Function
Program Counter	PC	Stores the sequence number of the next instruction to be executed. Also called Sequence Control Register (SCR).
Memory Address Register	MAR	Holds the memory address that contains either the next piece of data or an instruction that is to be used next.
Memory Data Register	MDR	Acts like a buffer holding anything being copied from the memory for processor's use. Also called MBR (Memory Buffer Register).
Arithmetic/Logic Unit	ALU	Handles all arithmetic and logical calculations. ALU is where data is processed.
Accumulator	ACC	A register that stores intermediate arithmetic and logic results. It is under direct control of ALU.
Control Unit	CU	Main component of the CPU. Manages the execution of the instructions.
Immediate Access Store	IAS	Location where data currently being worked on is stored.
Index Register	IR	Holds a number that is added to the memory field so that a range of address can easily be accessed.

3.3 Computer Architecture & Fetch-Execute Cycle

3.3.3 Fetch-Execute Cycle

•The Fetch-Execute cycle (also called fetch-decode-execute or fetch-decode-execute-reset cycle) is the process of fetching an instruction from the memory and executing it.
•This is done by the CPU with the help of the special registers.

1. Load the address that is in PC (Program Counter) into the MAR (Memory Address Register).
2. Increment PC by 1.
3. Load the instruction that is in the memory address given by the MAR into the MDR (Memory Data Register).
4. Load the instruction that is in MDR into the CIR (Current Instruction Register).
5. Decode the instruction that is in CIR.
6. If the instruction is a jump instruction then:
    1. Load the address part of the instruction into the PC.
    2. Reset by going to Step 1.
7. Execute the instruction.
8. Reset by going to Step 1.

3.3 Computer Architecture & Fetch-Execute Cycle

3.3.3 Fetch-Execute Cycle *(continued...)*

- Steps 1 to 4 are the Fetch part.
- Step 5 is the Decode part.
- Step 6 and 7 are the Execute part.

Note: Discussion of Index Register is pending.

3.3 Computer Architecture & Fetch-Execute Cycle

3.3.4 Parallel Processors

PARALLEL PROCESSORS

•Definition: The simultaneous use of more than one CPU or processor core to execute a program or multiple threads.

Advantages

•Ideally, parallel processing should make a program run faster as there are more than one CPU working on different portions of the program.

•This is specially useful in processor intensive programs such as simulations.

Disadvantages

•It is sometimes difficult to divide a program in such a way that separate CPUs can work on different portions without interfering with each other.

•The Operating System must also support the use of multiple processors and should know how to handle data and instruction from different portions of the program.

3.3.4 Parallel Processors *(continued…)*

ARRAY PROCESSOR

Definition: It is a central processor unit designed to allow any machine instruction to operate simultaneously on a number of data locations (data array).

Advantages

- Enables problems involving same calculations on a range of data to be solved very quickly.

Disadvantages

- Cannot be used in more general problem solving.

Example:

- Weather forecasting
- Simulations

3.3.4 Parallel Processors *(continued...)*

CO-PROCESSOR

Definition: A processor used to supplement the functions of the primary processor (the CPU).

- Operations performed by the coprocessor may be floating point arithmetic, graphics, signal processing, string processing, or encryption.

Advantages

- By offloading processor-intensive tasks from the main processor, coprocessors can accelerate system performance.

Disadvantages

- Adds to the cost of the computer.